FORM PTO-1390 (REV. 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 10191/2277
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO (If known, see 37 CFR 1 5) 10/070653

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	PRIORITY DATES CLAIMED
PCT/DE00/02918	(26 08.00) 26 August 2000	(08 09 99) 08 Sepember 1999

TITLE OF INVENTION

SEMICONDUCTOR ELEMENT AND METHOD OF MANUFACTURING THE SEMICONDUCTOR COMPONENT

APPLICANT(S) FOR DO/EO/US

SPITZ, Richard

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371
3. ☒ This express request to begin national examination procedures (35 U S C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U S C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date
5. ☒ A copy of the International Application as filed (35 U.S.C 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau)
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U S C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S C. 371(c)(4)). (unsigned)
10. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1 97 and 1.98.
12. ☐ An assignment document for recording A separate cover sheet in compliance with 37 CFR 3.28 and 3 31 is included.
13. ☒ A **FIRST** preliminary amendment.
    ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☒ A substitute specification and marked up version of substitute specification .
15. ☐ A change of power of attorney and/or address letter
16. ☒ Other items or information. Copies of International Search Report, Preliminary Examination Report and Form PCT/RO/101.

EXPRESS NO. EL594613017

U.S. APPLICATION NO. if known, see 37 C.F.R. 1.5	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
10/070653	PCT/DE00/02918	10191/2277

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO $890.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) $710.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $740.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1,040.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$890	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	8 - 20 =	0	X $18.00	$	
Independent Claims	2 - 3 =	0	X $84.00	$	
Multiple dependent claim(s) (if applicable)			+ $280.00	$	
TOTAL OF ABOVE CALCULATIONS =				$890	
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$890	
Processing fee of $130.00 for furnishing the English translation later the ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$890	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$	
TOTAL FEES ENCLOSED =				$890	
				Amount to be: refunded	$
				charged	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 11-0600 in the amount of **$890.00** to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-0600. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Kenyon & Kenyon
One Broadway
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By: [signature] Reg No 35,952
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Richard L. Mayer, Reg. No. 22,490
NAME

3/8/02
DATE

[10191/2277]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s)	:	Richard SPITZ
Serial No.	:	To Be Assigned
Filed	:	Herewith
For	:	SEMICONDUCTOR ELEMENT AND METHOD OF MANUFACTURING THE SEMICONDUCTOR COMPONENT
Examiner	:	To Be Assigned
Art Unit	:	To Be Assigned

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT AND

37 C.F.R. § 1.125 SUBSTITUTE SPECIFICATION STATEMENT

SIR:

Please amend the above-identified application before examination, as set forth below.

IN THE SPECIFICATION AND ABSTRACT:

In accordance with 37 C.F.R. § 1.121(b)(3), a Substitute Specification (including the Abstract, but without claims) accompanies this response. It is respectfully requested that the Substitute Specification (including Abstract) be entered to replace the Specification of record.

IN THE CLAIMS:

Please cancel original claims 1-15 and please cancel substitute claims 1-8, without prejudice.

Please add the following new claims:

EL594613017

9. (New) A method of manufacturing semiconductor components, the method comprising:

introducing depressions into a wafer of a first conductivity type;

coating both sides of the wafer with doping atoms;

carrying out a diffusion process;

dicing the wafer into individual chips so that, in an internal area, each of the chips has at least one depression; and

sawing the depressions.

10. (New) The method according to claim 9, wherein the depressions are formed as pits having a rectangular cross section.

11. (New) The method according to claim 9, further comprising applying metal layers to both sides of the wafer before the wafer is diced.

12. (New) The method according to claim 9, wherein the wafer is diced in areas of the wafer where no depressions have been introduced.

13. (New) The method according to claim 9, further comprising covering a top side of the wafer using a dopant of a second conductivity type.

14. (New) The method according to claim 9, further comprising covering a bottom side of the wafer using a dopant of the first conductivity type.

15. (New) The method according to claim 9, further comprising applying metal layers to first and third layers.

16. (New) A semiconductor component comprising:

a first layer of a first conductivity type having a top side and a bottom side, the first layer having areas of different thickness due to at least one depression introduced into the top side;

a second layer of a second conductivity type covering the top side of the first layer; and

a third layer situated on the bottom side of the first layer,

wherein the layers are diced into individual chips so that, in an internal area, each of the chips has at least one depression, and

wherein the depression is sawed.

REMARKS

This Preliminary Amendment cancels without prejudice original claims 1-15 and substitute claims 1-8, in the underlying PCT Application No. PCT/DE00/02918, and adds new claims 9-16. The new claims conform the claims to U.S. Patent and Trademark Office rules and do not add new matter to the application.

In accordance with 37 C.F.R. § 1.121(b)(3), the Substitute Specification (including the Abstract, but without the claims) contains no new matter. The amendments reflected in the Substitute Specification (including Abstract) are to conform the Specification and Abstract to U.S. Patent and Trademark Office rules or to correct informalities. As required by 37 C.F.R. § 1.121(b)(3)(iii) and § 1.125(b)(2), a Marked Up Version Of The Substitute Specification comparing the Specification of record and the Substitute Specification also accompanies this Preliminary Amendment. Approval and entry of the Substitute Specification (including Abstract) is respectfully requested.

The underlying PCT Application No. PCT/DE00/02918 includes an International Search Report, dated January 31, 2001. The Search Report includes a list of documents that were uncovered in the underlying PCT Application. A copy of the Search Report accompanies this Preliminary Amendment.

Applicant asserts that the present invention is new, non-obvious, and useful. Prompt consideration and allowance of the claims are respectfully requested.

Respectfully Submitted,

KENYON & KENYON

By: Reg No. 35,952

Dated: 3/8/02

By: _____
Richard L. Mayer
Reg. No. 22,490

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[10191/2277]

SEMICONDUCTOR ELEMENT AND METHOD OF MANUFACTURING THE SEMICONDUCTOR COMPONENT

Background Information

German Patent Application No. 36 33 161 describes a rectifier diode in which additional layout measures are provided in addition to a simple PN layer sequence to achieve an improved recovery behavior in commutation.

Summary Of The Invention

The arrangement according to the present invention and the method according to the present invention have the advantage over the related art that they make it possible to provide semiconductor components having high clock frequencies and thus short switching times without requiring additional layout measures and without a steep drop in the clearing current in reversal of polarity to the reverse direction. This ensures in a simple manner that despite short switching times, no steep current chopping will result in high interference voltage peaks due to the omnipresent leakage inductance; it is thus readily possible to use rapidly switching components in motor vehicles for rectifier configurations in which such voltage peaks would otherwise interfere with radio reception, for example. In addition, the diode according to the present invention guarantees a low forward voltage in addition to the short switching time and a gentle drop in the clearing current, and thus it also ensures low heat losses in polarization of the voltage applied to the component in the forward direction.

It is especially advantageous to provide pits having a rectangular cross section to produce the desired ratio between areas having different middle zone thicknesses using the smallest possible number of pits.

If the edge areas are formed by areas having no depressions, then the component is

insensitive to damage and contaminants at the edge of the chip.

Brief Description Of The Drawings

Figure 1 shows a rectifier diode.

Figure 2 shows a diagram.

Figure 3a shows a cross-sectional side view of a diode.

Figure 3b shows a top view of a diode.

Detailed Description

Figure 1 shows a diagram of a semiconductor diode having a weakly N-doped middle zone 2, which is covered with a strongly P-doped layer 1 on its top side and a strongly N-doped layer 3 on its bottom side. Layers 1 and 3 are provided with metallic coatings (not shown).

Layers 1 and 2 form the PN junction of the semiconductor diode at their common interface.

Figure 2 shows a diagram having a time axis 5 and an ordinate axis 6. This shows a sinusoidal curve 7 of the voltage applied to layers 1 and 3 of the semiconductor diode in Figure 1. In the forward direction, the current through the diode essentially follows voltage curve 7, i.e., the positive half-wave of voltage curve 7 in the left half of the diagram. If the polarity of voltage 7 changes, the diode is polarized in the reverse direction but the current through the diode still approximately follows the voltage curve for a short period of time, called switching time 9, until developing into clearing current curve 8.

In switching from forward direction to reverse direction, charge carriers induced into

the middle zone must be cleared out before the diode is capable of receiving the reverse voltage. The time required for this is switching time 9.

The cross-sectional side view in Figure 3a shows a layer sequence 10, 20, 30 which forms a diode. Layer 10 is N-doped and corresponds to the doping of a weakly N-doped substrate used in the manufacture of this component. A highly N-doped layer 20 applied to the bottom side of layer 10 is in turn provided with a metallic coating (not shown) on its outside. A strongly P-doped layer 30 is applied to the top side of layer 10. Pits 60 defining first areas 40 and second areas 50 are introduced into the top side of the diode. In first areas 40, layer 10 is thicker than in second areas 50, while layer 30 has approximately the same thickness in both areas. Pits 60 are situated in internal area 70 of the diode, while the remaining area of the diode, the edge area, is formed by first areas 40. A metallic coating (not shown) is again applied to surface 80 of the diode. In the top view in Figure 3b, cross-section line 100 marks the location for which the cross-sectional side view is illustrated in Figure 1a. On surface 80 can be seen pits 60 formed parallel to the outside edges of the diode, with the pits intersecting and two parallel pits running parallel to each outside edge of the component. The depth of pits 60 is approximately 70 micrometers, for example, while the thickness of layer 10 in area 40 is approximately 80 micrometers and the thickness of layer 10 in area 50 is approximately 10 micrometers. Layers 20 and 30 are each approximately 60 micrometers thick. The doping concentration in layer 10 amounts to approximately 4×10^{14} cm^{-3}, for example, and the doping concentration at the surfaces of layers 20 and 30 (the surface of layer 30 is labeled as 80 in Figure 3a) is approximately 7×10^{19} cm^{-3} each.

Area 40 is a highly blocking diode part having a broad middle zone 10 (breakdown voltage $\geq$ 200 volt), and area 50 is a highly blocking diode part (breakdown voltage $\geq$ 100 volt) having a narrow middle zone 10. Area 40 has a gentle clearing current drop because of the thick middle zone, while area 50 having the narrow middle zone results in a short switching time and a low forward voltage of the semiconductor

component according to the present invention. The edge area of the chip is formed by areas 40, so that the field strength at the edge of the chip remains low because of the higher breakdown voltage of areas 40 in comparison with areas 50. The diode is thus insensitive to damage and contaminants at the edge of the chip. If at least 25% of the forward current of the diode is flowing through areas 40, then an extremely gentle current drop is guaranteed after reversal of polarity of the voltage to the reverse direction of the diode.

In an alternative embodiment, the proportion of areas 50 of the total chip area is designed so that at least 50% of the current may flow through areas 50 to guarantee at the same time a gentle current drop for a very low forward voltage. This may be guaranteed through a corresponding number of pits or through a corresponding choice of the width of the pits. In addition to square chips, pentagonal, hexagonal or other polygonal chips may be provided with the pits according to the present invention arranged parallel to the respective edges of the chip and intersecting accordingly in a pentagonal, hexagonal or other polygonal pattern. The first type of conductivity is an N-type line, and the second type of conductivity is a P-type line. Of course, the selection may also be reversed. Semiconductor components other than diodes may also be provided with the pits according to the present invention in an advantageous manner. In particular in the case of diodes having three layers or four layers, i.e., transistor diodes or thyristor diodes, layers 30 and 10 then form the base-collector layers or the P and N layers of the middle PN junction.

The semiconductor diodes according to Figure 3 permit the implementation of higher clock frequencies due to their short switching times. Therefore, they are suitable in particular for use in automotive bridge rectifier configurations in which clock frequencies which are definitely above the frequencies of normal passive diode rectifiers are used. In the case of clocked rectifiers such as those described in German Patent Application No. 198 45 569.0, which was not published prior to the present application, clock frequencies of approximately 20 kHz may be achieved

with the semiconductor diodes described here having pits, which is approximately one order of magnitude higher than the conventional frequency of known automotive rectifier configurations, which is linked to the rate of rotation of the alternator and amounts to a maximum of approximately 2 kHz.

To manufacture a diode chip according to Figure 3, parallel pits 60 are first cut in a wafer having the doping of subsequent layer 10. Then strongly P-doped and strongly N-doped layers 30 and 20, respectively, are diffused into this wafer simultaneously. In another step, a metal layer is deposited on both sides of the wafer. The wafer is then divided into individual chips by cutting in another step, with the dividing lines running in areas 40 where middle zone 10 is thick in comparison with areas 50 where pits 60 have been produced. This chip may be soldered into known press-fit diode housing and sheathed with epoxy resin, for example.

To obtain largest possible areas 50, it is advantageous to cut the pits with rectangular profiles. The number of pits per chip is also determined from the fixed area proportions of area 40 to area 50 and from the selected pit width.

The method according to the present invention provides such components without additional diffusion layers and without additional layout measures. This is a method which is suitable for mass production and is also suitable for implementation outside of the clean room to some extent, at least with regard to producing the pits.

Abstract Of The Disclosure

A semiconductor component and a method of manufacturing it are described, making it possible to provide a switching element for high switching frequencies without the omnipresent leakage inductance resulting in high interference voltage peaks. Therefore, pits are produced in the surface of the wafer, resulting in a middle zone having a variable thickness laterally. First areas of this middle zone guarantee a gentle drop in clearing current, second areas guarantee short switching times and a low forward voltage.

(Figure 3a)

[10191/2277]

SEMICONDUCTOR ELEMENT AND METHOD OF MANUFACTURING THE SEMICONDUCTOR COMPONENT

Background Information

[The present invention relates to a semiconductor component and a method of manufacturing same according to the definition of the species of the independent claims.] German Patent Application No. 36 33 161 [A1] describes a rectifier diode in which additional layout measures are provided in addition to a simple PN layer sequence to achieve an improved recovery behavior in commutation.

[Advantages of the] Summary Of The Invention

The arrangement according to the present invention and the method according to the present invention [having the characterizing features of the independent claims] have the advantage over the related art that they make it possible to provide semiconductor components having high clock frequencies and thus short switching times without requiring additional layout measures and without a steep drop in the clearing current in reversal of polarity to the reverse direction. This ensures in a simple manner that despite short switching times, no steep current chopping will result in high interference voltage peaks due to the omnipresent leakage inductance; it is thus readily possible to use rapidly switching components in motor vehicles for rectifier configurations in which such voltage peaks would otherwise interfere with radio reception, for example. In addition, the diode according to the present invention guarantees a low forward voltage in addition to the short switching time and a gentle drop in the clearing current, and thus it also ensures low heat losses in polarization of the voltage applied to the component in the forward direction.

[Advantageous refinements of and improvements on the components and methods characterized in the independent claims are possible through the measures characterized in the dependent claims.]

MARKED-UP VERSION OF SUBSTITUTE SPECIFICATION

It is especially advantageous to provide pits having a rectangular cross section to produce the desired ratio between areas having different middle zone thicknesses using the smallest possible number of pits.

If the edge areas are formed by areas having no depressions, then the component is insensitive to damage and contaminants at the edge of the chip.

[Other advantages are derived from the features characterized in the description.

Drawing

Embodiments of the present invention are illustrated in the drawing and explained in greater detail in the following description.] Brief Description Of The Drawings

Figure 1 shows a rectifier diode[,].

Figure 2 shows a diagram[,].

Figure 3a shows a cross-sectional side view of a diode[, and].

Figure 3b shows a top view of a diode.

Detailed Description [of the Embodiments]

Figure 1 shows a diagram of a semiconductor diode having a weakly N-doped middle zone 2, which is covered with a strongly P-doped layer 1 on its top side and a strongly N-doped layer 3 on its bottom side. Layers 1 and 3 are provided with metallic coatings (not shown).

Layers 1 and 2 form the PN junction of the semiconductor diode at their common interface.

MARKED-UP VERSION OF SUBSTITUTE SPECIFICATION

Figure 2 shows a diagram having a time axis 5 and an ordinate axis 6. This shows a sinusoidal curve 7 of the voltage applied to layers 1 and 3 of the semiconductor diode in Figure 1. In the forward direction, the current through the diode essentially follows voltage curve 7, i.e., the positive half-wave of voltage curve 7 in the left half of the diagram. If the polarity of voltage 7 changes, the diode is polarized in the reverse direction but the current through the diode still approximately follows the voltage curve for a short period of time, called switching time 9, until developing into clearing current curve 8.

In switching from forward direction to reverse direction, charge carriers [indicated] induced into the middle zone must be cleared out before the diode is capable of receiving the reverse voltage. The time required for this is switching time 9.

The cross-sectional side view in Figure 3a shows a layer sequence 10, 20, 30 which forms a diode. Layer 10 is N-doped and corresponds to the doping of a weakly N-doped substrate used in the manufacture of this component. A highly N-doped layer 20 applied to the bottom side of layer 10 is in turn provided with a metallic coating (not shown) on its outside. A strongly P-doped layer 30 is applied to the top side of layer 10. Pits 60 defining first areas 40 and second areas 50 are introduced into the top side of the diode. In first areas 40, layer 10 is thicker than in second areas 50, while layer 30 has approximately the same thickness in both areas. Pits 60 are situated in internal area 70 of the diode, while the remaining area of the diode, the edge area, is formed by first areas 40. A metallic coating (not shown) is again applied to surface 80 of the diode. In the top view in Figure 3b, cross-section line 100 marks the location for which the cross-sectional side view is illustrated in Figure 1a. On surface 80 can be seen pits 60 formed parallel to the outside edges of the diode, with the pits intersecting and two parallel pits running parallel to each outside edge of the component. The depth of pits 60 is [approx.] approximately 70 micrometers, for example, while the thickness of layer 10 in area 40 is [approx.] approximately 80 micrometers and the thickness of layer 10 in area 50 is [approx.]

MARKED-UP VERSION OF SUBSTITUTE SPECIFICATION

approximately 10 micrometers. Layers 20 and 30 are each [approx.] approximately 60 micrometers thick. The doping concentration in layer 10 amounts to [approx.] approximately 4×10^{14} cm^{-3}, for example, and the doping concentration at the surfaces of layers 20 and 30 (the surface of layer 30 is labeled as 80 in Figure 3a) is [approx.] approximately 7×10^{19} cm^{-3} each.

Area 40 is a highly blocking diode part having a broad middle zone 10 (breakdown voltage $\geq$ 200 volt), and area 50 is a highly blocking diode part (breakdown voltage $\geq$ 100 volt) having a narrow middle zone 10. Area 40 has a gentle clearing current drop because of the thick middle zone, while area 50 having the narrow middle zone results in a short switching time and a low forward voltage of the semiconductor component according to the present invention. The edge area of the chip is formed by areas 40, so that the field strength at the edge of the chip remains low because of the higher breakdown voltage of areas 40 in comparison with areas 50. The diode is thus insensitive to damage and contaminants at the edge of the chip. If at least 25% of the forward current of the diode is flowing through areas 40, then an extremely gentle current drop is guaranteed after reversal of polarity of the voltage to the reverse direction of the diode.

In an alternative embodiment, the proportion of areas 50 of the total chip area is designed so that at least 50% of the current may flow through areas 50 to guarantee at the same time a gentle current drop for a very low forward voltage. This may be guaranteed through a corresponding number of pits or through a corresponding choice of the width of the pits. In addition to square chips, pentagonal, hexagonal or other polygonal chips may be provided with the pits according to the present invention arranged parallel to the respective edges of the chip and intersecting accordingly in a pentagonal, hexagonal or other polygonal pattern. The first type of conductivity is an N-type line, and the second type of conductivity is a P-type line. Of course, the selection may also be reversed. Semiconductor components other than diodes may also be provided with the pits according to the present invention in an

advantageous manner. In particular in the case of diodes having three layers or four layers, i.e., transistor diodes or thyristor diodes, layers 30 and 10 then form the base-collector layers or the P and N layers of the middle PN junction.

The semiconductor diodes according to Figure 3 permit the implementation of higher clock frequencies due to their short switching times. Therefore, they are suitable in particular for use in automotive bridge rectifier configurations in which clock frequencies which are definitely above the frequencies of normal passive diode rectifiers are used. In the case of clocked rectifiers such as those described in German Patent Application No. 198 45 569.0, which was not published prior to the present application, clock frequencies of [approx.] approximately 20 kHz may be achieved with the semiconductor diodes described here having pits, which is approximately one order of magnitude higher than the conventional frequency of known automotive rectifier configurations, which is linked to the rate of rotation of the alternator and amounts to a maximum of [approx.] approximately 2 kHz.

To manufacture a diode chip according to Figure 3, parallel pits 60 are first cut in a wafer having the doping of subsequent layer 10. Then strongly P-doped and strongly N-doped layers 30 and 20, respectively, are diffused into this wafer simultaneously. In another step, a metal layer is deposited on both sides of the wafer. The wafer is then divided into individual chips by cutting in another step, with the dividing lines running in areas 40 where middle zone 10 is thick in comparison with areas 50 where pits 60 have been produced. This chip may be soldered into known press-fit diode housing and sheathed with epoxy resin, for example.

To obtain largest possible areas 50, it is advantageous to cut the pits with rectangular profiles. The number of pits per chip is also determined from the fixed area proportions of area 40 to area 50 and from the selected pit width.

The method according to the present invention provides such components without

additional diffusion layers and without additional layout measures. This is a method which is suitable for mass production and is also suitable for implementation outside of the clean room to some extent, at least with regard to producing the pits.

MARKED-UP VERSION OF SUBSTITUTE SPECIFICATION

Abstract Of The Disclosure

A semiconductor component and a method of manufacturing it are described, making it possible to provide a switching element for high switching frequencies without the omnipresent leakage inductance resulting in high interference voltage peaks. Therefore, pits are produced in the surface of the wafer, resulting in a middle zone [(10)] having a variable thickness laterally. First areas [(40)] of this middle zone [(10)] guarantee a gentle drop in clearing current, second areas [(50)] guarantee short switching times and a low forward voltage.

(Figure 3a)

MARKED-UP VERSION OF SUBSTITUTE SPECIFICATION

4/prts

[10191/2277]

SEMICONDUCTOR ELEMENT AND METHOD OF MANUFACTURING THE SEMICONDUCTOR COMPONENT

Background Information

The present invention relates to a semiconductor component and a method of manufacturing same according to the definition of the species of the independent claims. German Patent Application 36 33 161 A1 describes a rectifier diode in which additional layout measures are provided in addition to a simple PN layer sequence to achieve an improved recovery behavior in commutation.

Advantages of the Invention

The arrangement according to the present invention and the method according to the present invention having the characterizing features of the independent claims have the advantage over the related art that they make it possible to provide semiconductor components having high clock frequencies and thus short switching times without requiring additional layout measures and without a steep drop in the clearing current in reversal of polarity to the reverse direction. This ensures in a simple manner that despite short switching times, no steep current chopping will result in high interference voltage peaks due to the omnipresent leakage inductance; it is thus readily possible to use rapidly switching components in motor vehicles for rectifier configurations in which such voltage peaks would otherwise interfere with radio reception, for example. In addition, the diode according to the present invention guarantees a low forward voltage in addition to the short switching time and a gentle drop in the clearing current, and thus it also ensures low heat losses in polarization of the voltage applied to the component in the forward direction.

Advantageous refinements of and improvements on the components and methods characterized in the independent claims are possible through the measures

characterized in the dependent claims.

It is especially advantageous to provide pits having a rectangular cross section to produce the desired ratio between areas having different middle zone thicknesses using the smallest possible number of pits.

If the edge areas are formed by areas having no depressions, then the component is insensitive to damage and contaminants at the edge of the chip.

Other advantages are derived from the features characterized in the description.

Drawing

Embodiments of the present invention are illustrated in the drawing and explained in greater detail in the following description. Figure 1 shows a rectifier diode, Figure 2 shows a diagram, Figure 3a shows a cross-sectional side view of a diode, and Figure 3b shows a top view of a diode.

Description of the Embodiments

Figure 1 shows a diagram of a semiconductor diode having a weakly N-doped middle zone 2, which is covered with a strongly P-doped layer 1 on its top side and a strongly N-doped layer 3 on its bottom side. Layers 1 and 3 are provided with metallic coatings (not shown).

Layers 1 and 2 form the PN junction of the semiconductor diode at their common interface.

Figure 2 shows a diagram having a time axis 5 and an ordinate axis 6. This shows a sinusoidal curve 7 of the voltage applied to layers 1 and 3 of the semiconductor diode in Figure 1. In the forward direction, the current through the diode essentially

follows voltage curve 7, i.e., the positive half-wave of voltage curve 7 in the left half of the diagram. If the polarity of voltage 7 changes, the diode is polarized in the reverse direction but the current through the diode still approximately follows the voltage curve for a short period of time, called switching time 9, until developing into clearing current curve 8.

In switching from forward direction to reverse direction, charge carriers indicated into the middle zone must be cleared out before the diode is capable of receiving the reverse voltage. The time required for this is switching time 9.

The cross-sectional side view in Figure 3a shows a layer sequence 10, 20, 30 which forms a diode. Layer 10 is N-doped and corresponds to the doping of a weakly N-doped substrate used in the manufacture of this component. A highly N-doped layer 20 applied to the bottom side of layer 10 is in turn provided with a metallic coating (not shown) on its outside. A strongly P-doped layer 30 is applied to the top side of layer 10. Pits 60 defining first areas 40 and second areas 50 are introduced into the top side of the diode. In first areas 40, layer 10 is thicker than in second areas 50, while layer 30 has approximately the same thickness in both areas. Pits 60 are situated in internal area 70 of the diode, while the remaining area of the diode, the edge area, is formed by first areas 40. A metallic coating (not shown) is again applied to surface 80 of the diode. In the top view in Figure 3b, cross-section line 100 marks the location for which the cross-sectional side view is illustrated in Figure 1a. On surface 80 can be seen pits 60 formed parallel to the outside edges of the diode, with the pits intersecting and two parallel pits running parallel to each outside edge of the component. The depth of pits 60 is approx. 70 micrometers, for example, while the thickness of layer 10 in area 40 is approx. 80 micrometers and the thickness of layer 10 in area 50 is approx. 10 micrometers. Layers 20 and 30 are each approx. 60 micrometers thick. The doping concentration in layer 10 amounts to approx. 4×10^{14} cm^{-3}, for example, and the doping concentration at the surfaces of layers 20 and 30 (the surface of layer 30 is labeled as 80 in Figure 3a) is approx. 7×10^{19} cm^{-3} each.

Area 40 is a highly blocking diode part having a broad middle zone 10 (breakdown voltage ≥ 200 volt), and area 50 is a highly blocking diode part (breakdown voltage ≥ 100 volt) having a narrow middle zone 10. Area 40 has a gentle clearing current drop because of the thick middle zone, while area 50 having the narrow middle zone results in a short switching time and a low forward voltage of the semiconductor component according to the present invention. The edge area of the chip is formed by areas 40, so that the field strength at the edge of the chip remains low because of the higher breakdown voltage of areas 40 in comparison with areas 50. The diode is thus insensitive to damage and contaminants at the edge of the chip. If at least 25% of the forward current of the diode is flowing through areas 40, then an extremely gentle current drop is guaranteed after reversal of polarity of the voltage to the reverse direction of the diode.

In an alternative embodiment, the proportion of areas 50 of the total chip area is designed so that at least 50% of the current may flow through areas 50 to guarantee at the same time a gentle current drop for a very low forward voltage. This may be guaranteed through a corresponding number of pits or through a corresponding choice of the width of the pits. In addition to square chips, pentagonal, hexagonal or polygonal chips may be provided with the pits according to the present invention arranged parallel to the respective edges of the chip and intersecting accordingly in a pentagonal, hexagonal or polygonal pattern. The first type of conductivity is an N-type line, and the second type of conductivity is a P-type line. Of course, the selection may also be reversed. Semiconductor components other than diodes may also be provided with the pits according to the present invention in an advantageous manner. In particular in the case of diodes having three layers or four layers, i.e., transistor diodes or thyristor diodes, layers 30 and 10 then form the base-collector layers or the P and N layers of the middle PN junction.

The semiconductor diodes according to Figure 3 permit the implementation of higher clock frequencies due to their short switching times. Therefore, they are suitable in particular for use in automotive bridge rectifier configurations in which clock

frequencies which are definitely above the frequencies of normal passive diode rectifiers are used. In the case of clocked rectifiers such as those described in German Patent Application 198 45 569.0, which was not published prior to the present application, clock frequencies of approx. 20 kHz may be achieved with the semiconductor diodes described here having pits, which is approximately one order of magnitude higher than the conventional frequency of known automotive rectifier configurations, which is linked to the rate of rotation of the alternator and amounts to a maximum of approx. 2 kHz.

To manufacture a diode chip according to Figure 3, parallel pits 60 are first cut in a wafer having the doping of subsequent layer 10. Then strongly P-doped and strongly N-doped layers 30 and 20, respectively, are diffused into this wafer simultaneously. In another step, a metal layer is deposited on both sides of the wafer. The wafer is then divided into individual chips by cutting in another step, with the dividing lines running in areas 40 where middle zone 10 is thick in comparison with areas 50 where pits 60 have been produced. This chip may be soldered into known press-fit diode housing and sheathed with epoxy resin, for example.

To obtain largest possible areas 50, it is advantageous to cut the pits with rectangular profiles. The number of pits per chip is also determined from the fixed area proportions of area 40 to area 50 and from the selected pit width.

The method according to the present invention provides such components without additional diffusion layers and without additional layout measures. This is a method which is suitable for mass production and is also suitable for implementation outside of the clean room to some extent, at least with regard to producing the pits.

Revised Claims

What is claimed is:

1. A method of manufacturing semiconductor components, depressions being introduced into a wafer of a first conductivity type; in a further step, both sides of the wafer being coated with doping atoms, and a diffusion process being carried out; and, in further step, the wafer being diced into individual chips, so that, in its internal area (70), each chip has at least one depression (60), wherein the depressions are sawed.

2. The method according to Claim 1, wherein the depressions are formed as pits having a rectangular cross section.

3. The method according to Claim 1 or 2, wherein metal layers are applied to both sides of the wafer before the wafer is diced.

4. The method according to one of the preceding claims, wherein the wafer is diced in areas (40) of the wafer where no depressions have been introduced.

5. The method according to one of the preceding claims, wherein a dopant of a second conductivity type is used in covering the top side.

6. The method according to one of the preceding claims, wherein a dopant of the first type of conductivity is used in covering the bottom side.

7. The method according to one of the preceding claims,

wherein the metal layers are applied to the first and the third layers.

8. A semiconductor component having a first layer (10) of a first conductivity type having a top side and a bottom side, the top side being covered by a second layer (30) of a second conductivity type, and a third layer (20) being situated on the bottom side, the first layer having areas (40, 50) of different thickness due to at least one depression (60) being introduced into the top side,
wherein the semiconductor component is manufactured in accordance with a method set forth in one of the preceding claims.

Abstract

A semiconductor component and a method of manufacturing it are described, making it possible to provide a switching element for high switching frequencies without the omnipresent leakage inductance resulting in high interference voltage peaks. Therefore, pits are produced in the surface of the wafer, resulting in a middle zone (10) having a variable thickness laterally. First areas (40) of this middle zone (10) guarantee a gentle drop in clearing current, second areas (50) guarantee short switching times and a low forward voltage.

(Figure 3a)

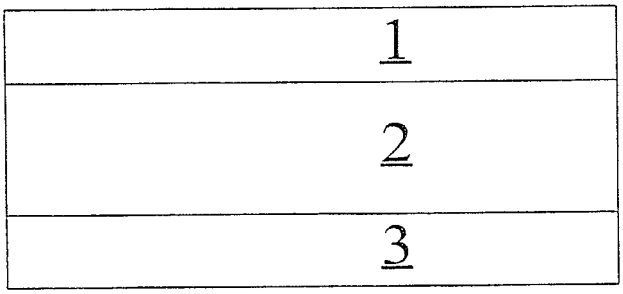

Fig.1

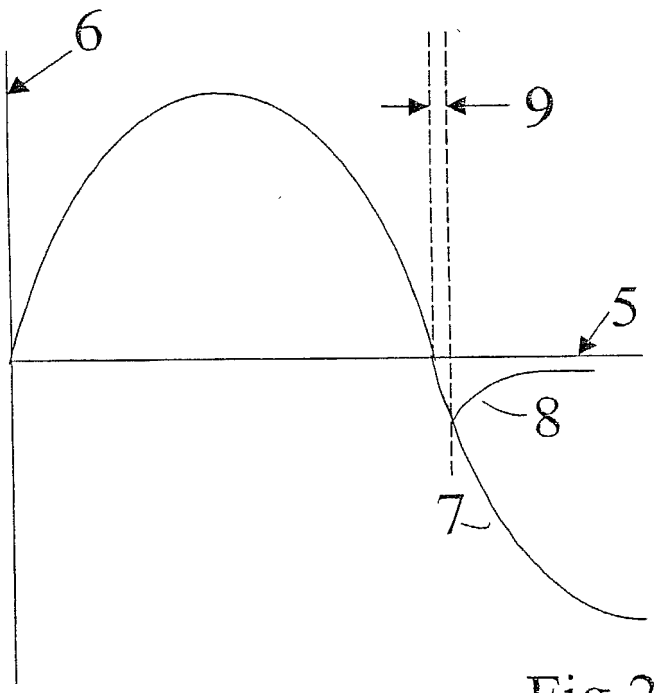

Fig.2

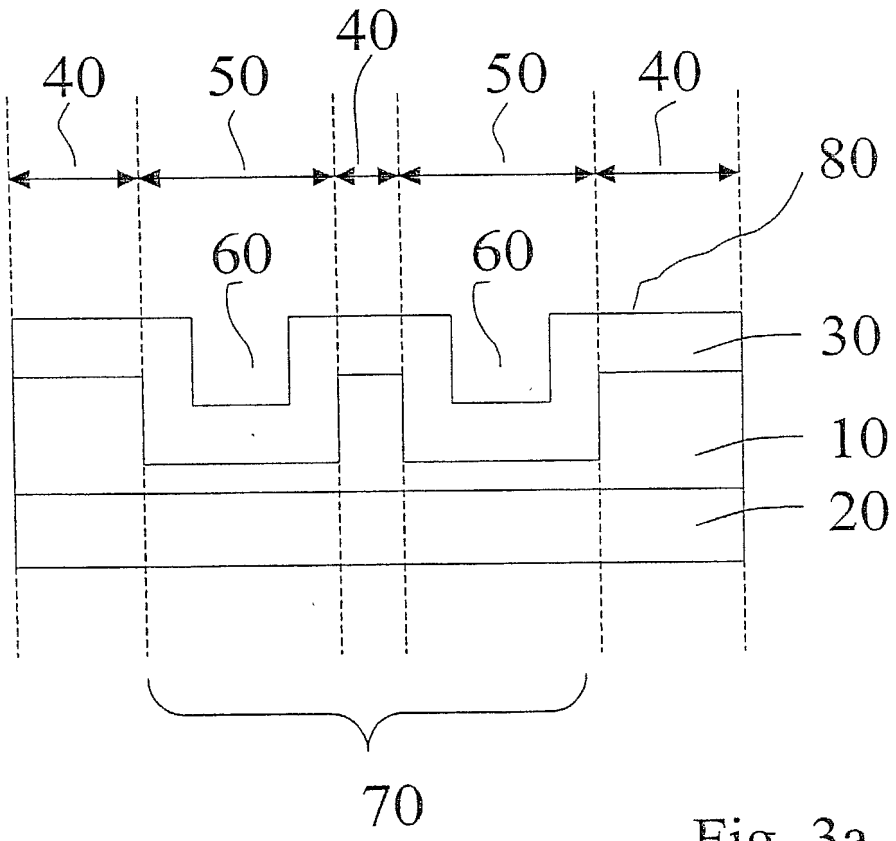

Fig. 3a

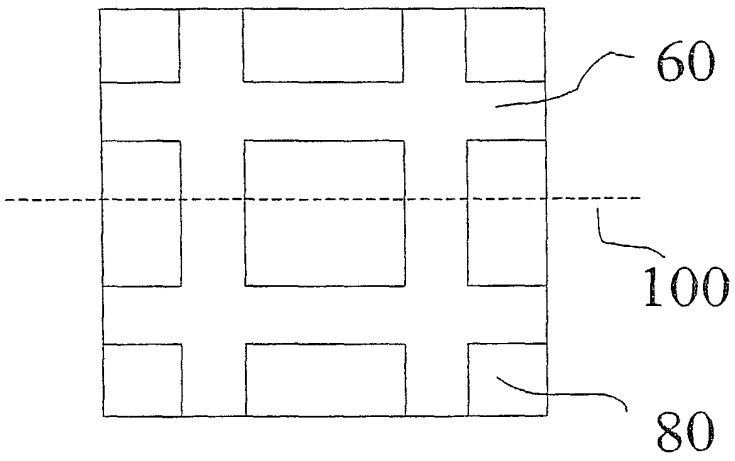

Fig. 3b

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **SEMICONDUCTOR ELEMENT AND METHOD OF MANUFACTURING THE SEMICONDUCTOR COMPONENT**, and the specification of which:

[ ] is attached hereto;

[ ] was filed as United States Application Serial No. _____ on _____, ____ and was amended by the Preliminary Amendment filed on _____, ____.

[X] was filed as PCT International Application Number PCT/DE00/02918 on the 26th day of August, 2000.

[X] an English translation of which is filed herewith.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a). I hereby claim foreign priority benefits under Title 35, United States Code § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international applications(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America

filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S)
AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119

Country : Germany

Application No. : 19942879.4

Date of Filing: September 8, 1999

Priority Claimed
Under 35 U.S.C. § 119 : [X] Yes [ ] No

I hereby claim the benefit under Title 35, United States Code § 120 of any United States Application or PCT International Application designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations § 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

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U.S. APPLICATIONS

Number :

Filing Date :

PCT APPLICATIONS
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PCT Number :

PCT Filing Date :

I hereby appoint the following attorney(s) and/or agents to prosecute

the above-identified application and transact all business in the Patent and Trademark Office connected therewith.

(List name(s) and registration number(s)):

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1-00

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